UNITED STATES PATENT AND TRADEMARK OFFICE

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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 February 2004</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-3,5-26,28,29 and 31-35</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-3, 5-26, 28, 29, and 31-35</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>06 February 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by

Applicant on May 21, 2002.

3.   Referring to claim 13, Oberman et al. have taught a method comprising:

a.   retrieving a pair of data elements from an array of elements in a single fetch

operation, wherein the pair of data elements includes an even data element and an odd

data element (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55,

line 14; page 55, line 31-page 56, line 18, elements 3182A, 3182B, 204A, 204C, Element

204A is the even data element and 204C is the odd data element.);

b.   substantially comparing the even element of the pair with an even extreme value

(Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53, line 20-page 55,

line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The element

204A is the extreme value that is compared with the even element 204C.);

c.   if the even element of the pair exceeds the even extreme value, storing the even

element of the pair as the even extreme value (Oberman et al., Figure 50, page 51, line 8-

page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18,

3182A, 3182B, 204A, 204C, The extreme value of elements 204A and 204C is stored in

3008A.);

d.   concurrent with said comparing the even element of the pair with the even

extreme value, comparing the odd element of the pair with an odd extreme value

(Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53, line 20-page 55,

line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The element

204B is the extreme value compared with the odd element 204D.);

e.   if the odd element of the pair exceeds the odd extreme value, storing the odd

element of the pair as the odd extreme value (Oberman et al., Figure 50, page 51, line 8-

page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18,

3182A, 3182B, 204A, 204C, The extreme value of elements 204B and 204D is stored in

3008B.).

4.   Oberman have not specifically taught substantially fetching and comparing remaining

pairs of data elements of the array until all of the data elements of the array have been processed.

However, with this limitation, applicant is merely claiming completing the work you begin. It

would have been obvious to anyone of ordinary skill in the art at the time the invention was

made to complete what you started.

5.   Referring to claim 14, Oberman et al. have taught the method of claim 13, as described

above, and further comprises setting the even extreme value as a function of the even element of

the element pair (Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53, line 20-

page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The extreme

value of elements 204A and 204C is stored in 3008A.) and setting the odd extreme value as a

function of the odd element of the element pair (Oberman et al., Figure 50, page 51, line 8-page

52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B,

204A, 204C, The extreme value of elements 204B and 204D is stored in 3008B.).

6.   Referring to claim 15, Oberman et al. have taught the method of claim 13, as described

above, and further comprises maintaining a first accumulator to store a minimum value for the

even elements (Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53, line 20-page

55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The extreme value of

elements 204A and 204C is stored in 3008A.) and a second accumulator to store a minimum

value for the odd elements (Oberman et al., Figure 50, page 51, line 8-page 52, line 11; page 53,

line 20-page 55, line 14; page 55, line 31-page 56, line 18, 3182A, 3182B, 204A, 204C, The

extreme value of elements 204B and 204D is stored in 3008B.).

7.   Claims 1, 2, 5, 6, 7, 8, 9, 10, 29, 31, 33, 34, and 35 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as

element "AA" in the IDS submitted by Applicant on May 21, 2002, in view of Oberman et al.,

WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on

May 21, 2002.

8.   Referring to claim 1, Kobayashi have taught a method comprising:

        a.   Receiving machine instructions directing a processor to search a plurality of N

        data elements (Kobayashi et al., abstract, column 2, lines 21-40, column 4, lines 5-15,

        column 5, lines 1-65); and

        b.   executing each machine instruction by:

        i.   retrieving M data elements in a single fetch cycle (Kobayashi et al.,

abstract, column 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65; when

M=1);

        ii.   concurrently comparing the M data elements to M corresponding current

extreme values (Kobayashi et al., abstract, column 2, lines 21-40, column 4, lines

5-15, column 5, lines 1-65, elements 3321 and 3322, where M=1); and

        iii.   updating a set of M references based on said comparing (Kobayashi et al.,

abstract, column 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65,

elements 3321 and 3322, where M=1).

9.   Kobayashi et al. have not specifically taught receiving a N/M machine instructions

directing a processor to search a plurality of N data elements, where N and M are integers greater

than one. However, Oberman has taught that the number of instructions are reduced for

performing a certain operation when two data elements are compared in parallel (Oberman, page

51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18).

With Oberman we have two separate things that used to be implemented with two instructions,

that are now implemented with one instruction (FPMIN and FPMAX). Implementing half as

many instructions of Kobayashi et al. is an obvious improvement in light of Oberman in order to

increase instruction level parallelism. For example, in the case of Oberman, M=2. If we have an

array of Kobayashi et al. of size 10, such that N=10, then 10/2=5 instructions would be required

to search the array. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have the invention of Kobayashi et al., receive N/M machine instructions

directing a processor to search a plurality of N data elements, where N and M are integers greater

than one, such that two times the amount of data is operated on in a single instruction, as taught

by Oberman, so that half as many instructions of Kobayashi et al. need to be received to search

an array for the desirable purpose of increasing instruction level parallelism and execution time.

10.   Referring to claim 2, Kobayashi et al. have taught the method of claim 1, as described

above, and wherein retrieving the M data elements comprises retrieving the M data elements as a

single data quantity containing the M data elements (Kobayashi et al., abstract, column 2, lines

21-40, column 4, lines 5-15, column 5, lines 1-65).

11.   Referring to claim 5, Kobayashi et al. in combination with Oberman have taught the

method of claim 1, wherein M = 2 and N is greater than two (Oberman, page 51, line 8-page 52,

line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18).

12.   Referring to claim 6, Kobayashi et al. have taught the method of claim 1, as described

above, and wherein executing each machine instruction further includes:

   a.   storing the current M extreme values in M accumulators (Kobayashi et al.,

   column 5, lines 1-65); and

   b.   copying the M data elements to the accumulators based on said comparing

   (Kobayashi et al., column 5, lines 1-65).

13.   Referring to claim 7, Kobayashi et al. in combination with Oberman have taught the

method of claim 5, as described above, and wherein concurrently comparing the M data elements

comprises processing a first data element with a first execution unit of a pipelined processor

(Oberman, page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-

page56, line 18, Figure 50, 136C/D) and processing a second data element with a second

execution unit of the pipelined processor (Oberman, page 51, line 8-page 52, line 11; page 53,

line 20-page 55, line 14; page 55, line 31-page56, line 18, Figure 50, 136C/D).

14.   Referring to claim 8, Kobayashi et al. in combination with Oberman have taught the

method. of claim 5, as described above, and wherein concurrently comparing the M data

elements comprises concurrently processing a first data element and a second data element

within a single execution unit of a pipelined processor (Oberman, page 51, line 8-page 52, line

11; page 53, line 20-page 55, line 14; page 55, line 31-page56, line 18, Figure 50, 136C, For the

FPMIN and FPMAX instructions, the pipelines each receive two operands to be compared.).

15.   Referring to claim 9, Kobayashi et al. in combination with Oberman have taught the

method of claim 1, as described above, and wherein concurrently comparing the M data elements

to M corresponding current extreme values includes determining whether each of the data

elements is less than the corresponding current extreme value (Kobayashi et al., abstract, column

2, line 21-40, column 4, lines 5-15, column 5, lines 1-65).

16.   Referring to claim 10, Kobayashi et al. in combination with Oberman have taught the

method of claim 1, as described above, and wherein concurrently comparing the M data elements

to M corresponding current extreme values includes determining whether each of the data

elements is greater than the corresponding current extreme value (Kobayashi et al., abstract,

column 2, line 21-40, column 4, lines 5-15, column 5, lines 1-65).

17.   Referring to claim 29, Kobayashi et al. in combination with Oberman et al. have taught

the limitations of claim 29, as described in the rejection to claims 11 and 12, and a processor

coupled to a memory device (Oberman, Figure 51, element 3404).

18.   Referring to claim 31, Kobayashi et al. in combination with Oberman et al. have taught

the system of claim 29, as described above, and wherein the pipeline includes M registers

configured to store the accumulators and pointers (Kobayashi, column 5, lines 44-65, temporary

register, Oberman, Figure 50, elements 3321 and 3322).

19.   Referring to claim 33, Kobayashi et al. in combination with Oberman have taught the

system of claim 31, as described above, and wherein the registers are general-purpose data

registers (Kobayashi, column 5, lines 44-65, temporary register, Oberman, Figure 50, elements

3321 and 3322).

20.   Referring to claim 34, Kobayashi et al. in combination with Oberman et al. have taught

the system of claim 29, as described above and wherein the memory device comprises static

random access memory (Oberman et al., Page 57, lines 3-5).

21.   Referring to claim 35, Kobayashi et al. in combination with Oberman et al. have taught

the system of claim 29. While Kobayashi et al. in combination with Oberman et al. may not have

taught wherein the memory device comprises FLASH memory, it is well known that flash

memory is connected to processors for the purpose of providing nonvolatile memory to maintain

data between sessions. Therefore it would have been obvious to one of ordinary skill in the art at

the time the invention was made to have the invention of Kobayashi et al. and Oberman et al.

include a flash memory connected to the processor for the desirable purpose of providing

nonvolatile memory to maintain data between sessions.

22.   Claim 3, 11, 12, 19, 20, 21, 22, 23, 24, 25, 26, 28, and 32 are rejected under 35 U.S.C.

103(a) as being unpatentable over Kobaysashi et al., US Patent 4,774,688, cited in paper number

3, as element "AA" in the IDS submitted by Applicant on May 21, 2002, in view of Oberman et

al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002, and in view of Stroustrup.

23.   Referring to claim 3, Kobayashi et al. in view of Oberman have taught the method of claim 2, as described above. Kobayashi have not specifically taught wherein the set of M references comprise pointer registers to store addresses of extreme data quantities in the array of N data elements. However Stroustrup has taught that a set of references comprise pointer registers to store addresses for data quantities (Stroustrup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays") in order to efficiently and elegantly handle traversing an array. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of references, as taught by Kobayashi et al., comprise pointer registers to store addresses for data, as taught by Stroustrup (Stroustrup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays"), for the desirable purpose of efficiently and elegantly searching arrays.

24.   Referring to claim 11, Kobayashi et al. have taught a method for searching an array of N data elements for an extreme value (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65), the method comprising:

   a.   issuing machine instructions to a processor (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65);

   b.   executing each machine instruction by:

      i.   retrieving M data elements in a single fetch cycle (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65, When M=1);

      ii.   concurrently comparing the M data elements to corresponding M current

extreme values (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines

5-15, column 5, lines 1-65, elements 3321 and 3322, Where M=1), and

      iii.   updating accumulators associated with the M current extreme values based

on said comparing (Kobayashi et al., abstract, column, 2, lines 21-40, column 4,

lines 5-15, column 5, lines 1-65, Where M=1.); and

25.   analyzing results of the machine instructions to identify the extreme value in the array

(Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65,

Identify a minimum or maximum value.).

26.   Kobayashi et al. have not specifically taught issuing N/M machine instructions to a

processor, wherein the processor is adapted to process M data elements in parallel.

27.   Oberman has taught issuing machine instructions to a processor, wherein the processor is

adapted to process M data elements in parallel (Oberman et al., page 51, line 8-page 52, line 11;

page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18). It would have been obvious

to one of ordinary skill in the art at the time the invention was made to have the invention of

Kobayashi et al. include wherein the processor is adapted to process M data elements in parallel,

as taught by Oberman, in order to increase parallelism per instruction which speeds up execution

time.

28.   While Kobayashi et al. may not have specifically taught issuing N/M machine

instructions to a processor, Oberman has taught that the number of instructions are reduced for

performing a certain operation when two data elements are compared in parallel. With Oberman

we have two separate things that used to be implemented with two instructions that are now

implemented with one instruction (FPMIN and FPMAX). Implementing half as many

instructions of Kobayashi et al. is an obvious improvement in light of Oberman in order to

increase instruction parallelism. For example, in the case of Oberman, M=2. If we have an array

of Kobayashi of size 10, such that N=10, then 10/2 = 5 instructions would be required to search

the array for an extreme value. It would have been obvious to one of ordinary skill in the art at

the time the invention was made to have the invention of Kobayashi et al., issue N/M machine

instructions to a processor, such that 2 times the amount of data is operated on in a single

instruction, as taught by Oberman et al., so that ½ as many instructions of Kobayashi et al. need

to be issued to search an array for an extreme value for the desirable purpose of increasing

instruction level parallelism and execution time.

29.   Kobayashi et al. have not specifically taught updating pointers associated with the M

current extreme values based on said comparing. However, Stroustrup has taught updating

pointers (Stroustrup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays") in order to

efficiently and elegantly handle traversing an array. It would have been obvious to one of

ordinary skill in the art at the time the invention was made to update pointers, as taught by

Stroustup, in the invention of Kobayashi et al., for the desirable purpose of efficiently and

elegantly searching the array to find the extreme value.

30.   Referring to claim 12, Kobayashi et al. in combination with Oberman and Stroustrup

have taught the method of claim 11, as described above, and further comprising: setting up

registers for accumulators (Kobayashi et al., abstract, column, 2, lines 21-40, column 4, lines 5-

15, column 5, lines 1-65, Where M=1.) and pointers (Stroustrup, Pages 92-93, section 5.3.1

entitled "Navigating Arrays").

31.   Claim 19 does not claim anything over claim 11 and is therefore rejected for the same reasons as claim 11.

32.   Claim 20 does not claim anything over claim 12 and is therefore rejected for the same reasons as claim 12.

33.   Claim 21 does not claim anything over claims 11 and 12 and is therefore rejected for the same reasons as claims 11 and 12.

34.   Claim 22 does not claim anything over claim 3 and is therefore rejected for the same reasons as claim 3.

35.   Referring to claim 23, Oberman et al. have taught the apparatus of claim 21, as described above and wherein the registers are general-purpose data registers (Oberman et al., page 51, line 8-page 52, line 11; page 53, line 20-page 55, line 14; page 55, line 31-page 56, line 18, Figure 50, 3008A and 3008B).

36.   Referring to claim 24, Oberman et al. have taught the apparatus of claim 19, as described above, and wherein the pipeline includes M accumulators to store M current extreme values (Figure 50, elements 3008A and 3008B).

37.   Referring to claim 25, Oberman et al. have taught the apparatus of claim 19, as described above and wherein the pipeline includes M general-purpose registers to store M current extreme values (Figure 50, elements 3008A and 3008B).

38.   Claim 26 does not claim anything over claims 11 and 12 and is therefore rejected for the same reasons as claims 11 and 12.

39.   Claim 28 does not claim anything over claim 8 and is therefore rejected for the same reasons as claim 8.

40.   Claim 32 does not claim anything over claim 3 and is therefore rejected for the same

reasons as claim 3.

41.   Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by

Applicant on May 21, 2002, in view of Stroustrup.

42.   Referring to claim 16, Oberman et al. a have taught he method of claim 13, as described

above.   Oberman has taught storing an extreme value of the even data elements (Oberman et al.,

Figure 50, 3008A) and storing an extreme value of the odd elements (Oberman et al., Figure 50,

3008B). Oberman et al. have not specifically taught further including maintaining a first pointer

register to store an address for the extreme value of the even data elements and maintaining a

second pointer register to store an address for the extreme value of the odd data elements.

43.   However, Stroustroup has taught referencing data values using a pointer register while

accessing an array (Stroustroup, Pages 92-93, section 5.3.1 entitled "Navigating Arrays") in

order to efficiently and elegantly handle reference a value in an array of values. Therefore it

would have been obvious to one of ordinary skill in the art at the time the invention was made to

have the odd and even minimum values of Oberman et al. be referenced by an address pointer, as

taught by Stroustroup, in order to efficiently and elegantly maintain a value in an array of values.

44.   Referring to claim 17, Oberman et al. have taught the method of claim 16, as described

above, and further including adjusting at least one of the pointer registers after processing all of

the pairs of data elements to account for a number of stages in a pipeline (Figure 50, The output

results, elements 3008A and 3008B are adjusted, or set, after elements 204A-D are finished

being compared in the required number of pipeline stages necessary to complete the comparison.).

45.   Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman et al., WO 9923548, cited in paper number 3, as element "AJ" in the IDS submitted by Applicant on May 21, 2002, in view of Kobaysashi et al., US Patent 4,774,688, cited in paper number 3, as element "AA" in the IDS submitted by Applicant on May 21, 2002.

46.   Referring to claim 18, Oberman et al. have taught the method of claim 13, as described above. Oberman et al. have not specifically taught wherein the method is invoked by issuing N/M machine instructions to a programmable processor, wherein N equals a number of elements in the array, and M equals a number of data elements that the processor can concurrently compare. Kobayashi et al. have taught comparing an array of N data elements to find an extreme value (Kobayashi et al., abstract, column 2, lines 21-40, column 4, lines 5-15, column 5, lines 1-65). While Kobayashi et al. may not have specifically taught issuing N/M machine instructions to a processor, Oberman has taught that the number of instructions are reduced for performing a certain operation when two data elements are compared in parallel. With Oberman we have two separate things that used to be implemented with two instructions, that are now being implemented with one instruction (FPMIN and FPMAX). Implementing half as many instructions of Kobayashi et al. is an obvious improvement in light of Oberman in order to increase instruction parallelism. For example, in the case of Oberman, M=2. If we have an array of Kobayashi of size 10, such that N=10, then 10/2 = 5 instructions would be required to search the array for an extreme value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Kobayashi et al., issue N/M machine

instructions to a processor, such that 2 times the amount of data is operated on in a single

instruction, as taught by Oberman et al., so that ½ as many instructions of Kobayashi et al. need

to be issued to search an array for an extreme value for the desirable purpose of increasing

instruction level parallelism and execution time.

Response to Arguments

47.   Applicant's arguments with respect to claims 1-3, 5-26, 28, 29, and 31-35   have been

considered but are moot in view of the new ground(s) of rejection.

Conclusion

48.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

49.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this
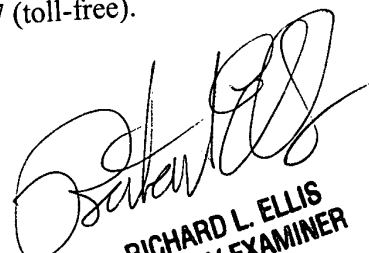
final action.

50.   Any inquiry concerning this communication or earlier communications from the examin

er should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The

examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

Application/Control Number: 09/675,066
Art Unit: 2183

51.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

52.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

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RICHARD L. ELLIS
PRIMARY EXAMINER